SINGLE METAL PIXEL ARRAY FOR LIGHT VALVE
UTILIZING LATERAL SUBLITHOGRAPHIC SPACER ISOLATION

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BACKGROUND OF THE INVENTION

5   1.   FIELD OF THE INVENTION

The present invention relates to light valves, and in particular, to pixel cell arrays for light valves which utilize sublithographic isolation based upon the formation of dielectric spacer structures.

10   2.   DESCRIPTION OF THE RELATED ART

Liquid crystal displays (LCDs) are becoming increasingly prevalent in high-density projection display devices. These display devices typically include a light source which passes light through a
15   light valve.

One of the methods for producing colors in a liquid crystal display is to sequentially project light having a wavelength corresponding to a primary color onto a single light valve. Color sequential
20   light valves create a spectrum of color within the range of the human perception by switching between a set of discrete primary colors. Typically, red, green, and blue are the primary tri-stimulus colors used to create the remaining colors of the spectrum.
25   Specifically, during projection of each primary color, the light intensity is modulated such that combination of the intensities of the primary colors in sequence produces the desired color. The frequency of switching between the primary
30   wavelengths by the light valve should be sufficiently

rapid to render discrete primary states
indistinguishable to the human eye.

Two factors dictate the minimum frequency
necessary for switching. The first factor is the
ability of the human eye to detect the discrete
primary colors (e.g., red, green, blue). At slower
than ideal switching speeds, the human eye will
detect a flicker and the primaries may not blend.

The second factor determining the frequency of
switching is the video refresh rate. During display
of video images, the individual frames must be
refreshed at frequencies undetectable to the human
eye.

The net frequency of switching demanded by the
combination of sequential color blending and video
refreshing is beyond the capabilities of light valves
that utilize thick (> 1μm) liquid crystal (LC)
transducers. However, thin (< 1μm) liquid crystal
transducers have been successfully fabricated. These
thin LC transducers demonstrate adequate color
sequential blending at video refresh rates. One
example of such a thin LC transducer pixel cell
structure is disclosed in US Patent No. 5,706,067, to
Colgan et al.

In general, the conventional thin LC transducer
pixel cells possess enhanced responsiveness due to
the decreased volume of liquid crystal material
between the top and bottom plates. A smaller volume
enables the liquid crystal to shift orientation more
quickly and in response to a lower applied voltage.

FIG. 1 shows a cross-sectional view of adjacent
thin LC transducer pixel cells in a conventional
light valve. Light valve portion 100 comprises
adjacent pixel cells 110a and 110b having liquid

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crystal (LC) material 111 sandwiched within gap 106 between a top plate and a bottom plate. Top plate 102 is composed of a translucent material, typically glass. The bottom plate is formed by the reflective

5   metal pixel electrodes 112a and 112b of adjacent pixels 110a and 110b, respectively.

Pixel electrodes 112a and 112b are separated and electrically isolated by trench 118. Pixel electrodes 112a and 112b lie on top of an upper

10   intermetal dielectric layer 128 that is one component of interconnect scheme 104. Interconnect 104 overlies capacitor structures 118a and 118b formed within underlying silicon substrate 105. Underlying capacitors 118a and 118b are in electrical

15   communication with pixel electrodes 112a and 112b, respectively, through metal-filled vias 140 and middle interconnect metallization layer 124 and lower interconnect metallization layer 122.

FIGS. 2AA-2DB illustrate the steps of the

20   conventional process for forming an array of pixel cells in a light valve. For purposes of convention, all FIGS. 2_A illustrate a top view of the pixel cell, all FIGS. 2_B illustrate a cross-sectional view of the pixel cell along line A-A' of the FIG. 2_A.

25   FIGS. 2AA-2AB illustrate the starting point for the conventional process for fabricating a thin LC transducer pixel cell. Starting structure 200 is created by forming an upper intermetal dielectric layer 212 over a lower interconnect metallization

30   layer 214. A central portion of upper intermetal dielectric layer 212 is then etched to form via 216. A liner (not shown) typically composed of a Ti/TiN layer combination, is then formed on the walls of via 216, and via 216 is filled with metal (typically CVD

Tungsten). Excess metal is then removed from the
surface of upper dielectric layer 212, typically by a
combination of etching and chemical-mechanical
polishing (CMP).

5   FIGS. 2BA-2BB illustrate formation of the metal
pixel electrode in accordance with the conventional
process. Metal pixel electrode layer 206 is formed
over the entire surface of the pixel cell.

FIGS. 2CA-2CB illustrate patterning of a
10   photoresist mask 207 over pixel electrode layer 206.
FIGS. 2DA-2DB show the etching of regions of pixel
electrode layer 206 unmasked by photoresist 207, to
form a plurality of intersecting trenches 218,
followed by stripping of photoresist mask 207.
15   Intersecting trenches 218 in turn define a plurality
of discrete pixel cell electrodes 230.

Fabrication of the thin LC transducer pixel cell
is completed by forming an alignment surface (not
shown) for the LC material positioned on top of the
20   pixel electrode. Forming this alignment surface is a
two step process. First, a dielectric film
(typically polyimide) is deposited on top of the
pixel electrode. Second, the dielectric film is
scored by a rubbing wheel, which traverses the
25   surface of the pixel cell and gouges the alignment
surface in a uniform direction. Liquid crystal
material is then placed within the cell, and a top
glass plate is secured to the tops of the support
pillars.

30   The conventional fabrication process described
above in FIGS. 2AA-2DB is adequate to produce
functional thin LC transducer pixel cells. However,
the conventional process flow suffers from a number
of disadvantages.

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One problem is that the step of defining and *additional masking step*
etching the inter-pixel trenches requires an
additional masking step. This masking step carries
with it penalties in terms of additional defects and
5   higher cost.

Another problem is that the minimum spacing
between adjacent pixels is dictated by the limits of
resolution of the photolithographic process employed.
This limitation is manifested in the step of
10   patterning the mask to form the trenches in the pixel
electrode layer, as shown above in FIG. 2CA-2CB. For
example, in a 0.3μm linewidth photolithographic
technology, the distance across trench 218 of
FIGS. 2DA-DB could be no less than 0.3μm.

15   The closer together the pixels of the array, the
better the array will perform. This is particularly
true with respect to minimizing leakage of incident
light between pixel electrodes through the
interconnect and into the underlying substrate, as
20   there is less inter-pixel spacing to allow the
passage of incident light. Close proximity between
pixels also reduces unwanted optical artifacts
attributable to interruption in the continuous pixel
array backplane by topography of inter-pixel
25   isolation structures.

Therefore, there is a need in the art for a
process of forming an array of pixel cells where
inter-pixel spacing between pixels is not constrained
by photolithographic parameters, thereby enabling
30   formation of arrays having greater pixel cell
densities and enhanced resolution and clarity.

SUMMARY OF THE INVENTION

The present invention provides a process flow for forming an array of pixel cells that does not rely upon photolithography to define inter-pixel isolation. Instead, adjacent pixels of the array are electrically insulated from one another by dielectric spacer structures formed by the deposition and etching of a dielectric layer conforming to raised features of a sacrificial layer. The thickness of the sidewall spacers is determined by the conditions under which the dielectric material forming the spacers is deposited. The deposition rate of dielectric material can be carefully controlled to produce spacers having a thickness of substantially less than the minimum line width of a given photolithography system. In this manner, inter-pixel isolation in accordance with the present invention can result in fabrication of pixel arrays having much greater cell densities than found in conventional arrays.

A process flow for forming a pixel cell array in accordance with one embodiment of the present invention comprises the steps of forming a sacrificial layer on top of an upper intermetal dielectric layer, forming a photoresist mask over the sacrificial layer in a checkerboard pattern which includes a plurality of masked squares but which excludes corners of the masked squares, and etching unmasked portions of the sacrificial layer to stop on the upper intermetal dielectric layer to leave a raised portion of the sacrificial layer having a top and sidewalls. The photoresist mask is removed, and a first dielectric layer is formed over the upper intermetal dielectric layer and the top of the

sacrificial layer, the first dielectric layer
conforming to the sidewalls. The first dielectric
layer is then etched to remove the first dielectric
layer over the upper intermetal dielectric layer

5   while leaving vertical dielectric spacer structures
along the sidewalls. The raised portions of the
sacrificial layer are then removed to leave the
dielectric spacer structures, and a metal layer is
formed over the upper intermetal dielectric layer and

10   the dielectric spacer structures. The metal layer is
then subjected to chemical-mechanical polishing to
form a substantially planar metal electrode surface
including intervening dielectric structures.

        An apparatus in accordance with one embodiment

15   of the present invention comprises an array of pixel
cells arranged in a checkerboard pattern having a
first set of squares alternating with a second set of
squares, the first set of squares and the second set
of squares formed from a first metal layer and

20   lacking corners, and further comprises dielectric
spacer structures having a thickness intervening
between the first set of squares and the second set
of squares.

        The features and advantages of the present

25   invention will be understood upon consideration of
the following detailed description of the invention
and the accompanying drawings.

                    BRIEF DESCRIPTION OF THE DRAWINGS
        FIG. 1 shows a cross-sectional view of adjacent

30   pixel cells in a conventional light valve.
        FIGS. 2AA-2DB show top and cross-sectional views
of the conventional process steps for forming an
array of pixel cells.

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FIG. 3 shows a cross-sectional view of a conventional CMOS gate structure.

FIGS. 4AA-4HB show top and cross-sectional views of the process steps for forming an array of pixel
5   cells in accordance with a first embodiment of the present invention.

FIG. 5 shows a plan view of a photoresist mask in accordance with a first alternative embodiment of the present invention.

10   FIG. 6 shows a plan view of a photoresist mask in accordance with a second alternative embodiment of the present invention.

FIG. 7 shows a cross-sectional view of a chemical-mechanical polishing step in accordance with
15   an alternative embodiment of the present invention.

DETAILED DESCRIPTION

The increasing reliance upon digital integrated circuit technology has heightened the importance of ensuring that process flows leading to formation of
20   pixel arrays are compatible with those leading to formation of CMOS devices. One characteristic feature of CMOS process flows is formation of dielectric spacer structures on either side of the polysilicon gate.

25   FIG. 3 shows a cross-sectional view of an exemplary CMOS gate structure. First, gate 300 is formed over single crystal silicon 302 to define a channel region 302a. Gate 300 consists of polysilicon layer 304 overlying gate oxide layer 306.

30   Lightly-doped drain (LDD) regions 308 are then implanted into single crystal silicon 302, aligned to the edge of gate 300. Dielectric spacer structures 310 are then formed adjacent to gate 300. Spacer

structures 310 are created by forming a dielectric layer that conforms to vertical sidewalls 300a of gate 300, and then carefully etching the dielectric layer to leave only spacer structures 310.

Finally, source/drain regions 312 are implanted into single crystal silicon 312, aligned to spacer structures 310. Source/drain regions 312 are linked to channel 302a by LDD regions 308.

The length of the gate (L_G) is the defining feature of a CMOS device. In general, the minimum linewidth capability of a given photolithography system thus generally defines L_G. In many photoresist systems, the thickness of the spacers (L_S) is typically substantially less than the gate length.

Therefore, the present invention utilizes dielectric spacer structures to accomplish sublithographic electrical isolation of adjacent electrodes of a pixel array. In this process, a sacrificial layer is deposited over an upper intermetal dielectric and then etched to form a checkerboard pattern. A dielectric layer conforming to the underlying surface is deposited and then carefully etched to leave only spacer structures along sidewalls of raised portions of the sacrificial layer.

The sacrificial layer is then removed, leaving only the dielectric spacer structures above the intermetal dielectric layer. A metal layer is formed over the entire surface, and a thin dielectric layer is formed over the metal layer. The thin dielectric layer and metal layer are subjected to chemical-mechanical polishing, such that exposed tops of the dielectric spacer structures separate and electrically isolate electrodes of adjacent pixel cells.

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FIGS. 4AA-4HB illustrate the process steps for forming an array of pixel cells in a light valve in accordance with a first embodiment of the present invention. For purposes of convention, all FIGS. 4A

5   illustrate a top view of the pixel cell array, and all FIGS. 4B illustrate a cross-sectional view of the pixel cell array along line A-A' of the FIG. 4A.

FIGS. 4AA-4AB illustrate the starting point for the process. Upper intermetal dielectric layer 402

10   is formed over upper interconnect metallization layer 400. Vias 404 are etched through upper intermetal dielectric layer 402 to stop on upper interconnect metallization layer 400. Vias 404 are filled with metal, and excess metal is removed.

15   FIGS. 4BA-4BB show the next step, wherein sacrificial layer 406 is formed over the entire surface. FIGS. 4CA-4CB show patterning of a photoresist layer, followed by development of the photoresist to form first photoresist mask 410.

20   Sacrificial layer 406 is then etched in unmasked regions.

In FIG. 4CA, photoresist mask 410 is shown in the form of a slightly modified checkerboard, with corners 410a excluded. As described in detail below,

25   exclusion of corners 410a from first mask 410 creates gap 411 having a width Z between adjacent diagonally-situated pixels. Subsequent formation of dielectric material within gap 411 prevents electrical contact between the tips of the diagonally-situated

30   electrodes, thereby ensuring adequate inter-pixel isolation.

FIGS. 4DA-4DB show stripping of photoresist mask 410, followed by formation of dielectric layer 412 over the entire surface, including raised portions of

sacrificial layer 406. Dielectric layer 412 conforms
closely to the underlying topography, becoming
vertical along raised sidewalls 406a of sacrificial
layer 406. Careful control over the rate of chemical
5   vapor deposition of dielectric material during this
step can result in the formation of spacer walls
substantially narrower than the minimum linewidth of
a given photolithography system.

In order to ensure proper electrical isolation
10   between diagonally-situated pixel electrodes, the
combined thickness of the dielectric material formed
on opposing sides of gap 411 must be greater than the
width Z of gap 411. Assuming an equal rate of
deposition on both sides of gap 411, the thickness of
15   dielectric layer 411 must therefore be at least ½Z,
and preferably larger.

FIGS. 4EA-4EB show anisotropic etching of
dielectric layer 412. This etching is carefully
controlled, so that dielectric layer 412 is
20   completely removed over the surface of upper
intermetal dielectric 402 and vias 404, but remains
along sidewalls 406a of raised portions of
sacrificial layer 406 as dielectric spacer structures
414. Dielectric spacer structures 414 have a curved
25   upper portion 414a reflecting the shape of dielectric
layer 412 as originally deposited.

FIGS. 4FA-4FB show the next step in the process
flow, wherein sacrificial layer 406 is removed to
leave only dielectric spacer structures 414
30   projecting from upper intermetal dielectric layer
402.

Next, in FIG. 4GA-4GB, metal layer 416 is formed
over the entire surface, and second dielectric layer
418 is formed over metal layer 416.

FIGS. 4HA-4HB show chemical-mechanical polishing through the second dielectric layer into the metal layer. Chemical-mechanical polishing extends into upper curved portion 414a of dielectric spacer structure 414. The result of this chemical-mechanical polishing is formation of adjacent pixel electrodes 415 electronically isolated by intervening dielectric spacers 414.

Fabrication of the liquid crystal silicon light valve is completed by adding liquid crystal material, and then sealing a translucent top plate over the structure.

The thin LC transducer pixel cell and the process for forming this pixel cell in accordance with the present invention offers a number of important advantages. One advantage is that an array is formed having a high density of pixel cells. Because inter-pixel spacing can be reduced below limits imposed by photolithographic constraints, the present invention permits pixel electrodes to readily be positioned closer together than previously possible given a particular photolithography system. Closer spacing of pixels in turn permits finer resolution of images, and minimizes distortion caused by interruption in the otherwise continuous reflective backplane of the light valve attributable to inter-pixel topography. Closer pixel spacing also helps prevent unwanted leakage of light in the space between pixels.

Co-pending, commonly assigned United States Patent Application S.N. __/___,___, entitled "Double-Metal Pixel Array for Light Valve Utilizing Lateral Sublithographic Spacer Isolation" (hereafter "the Co-pending Application") is hereby incorporated by

reference. The Co-pending Application discloses a
pixel array and a process for forming the array that
is similar to the present invention. Specifically, a
first metal layer is etched according to the
5   checkerboard pattern, and then dielectric spacers are
formed on sidewalls of the remaining raised features
of the first metal layer. A second metal layer is
then formed on top of the entire surface. Chemical-
mechanical polishing reveals a pixel array consisting
10   of alternating squares of the first and second metal
layers.

The present invention also offers several
advantages over the Co-pending Application.
Specifically, in the Co-pending Application the
15   thickness of the first metal layer and hence the
height of the spacers is dictated by the requirements
of the reflective electrode. Thus, the first metal
layer may be required to have a certain minimum
thickness that in turn limits the minimum spacing
20   between adjacent pixel cells.

By contrast, in the present invention the spacer
structures are formed on the sidewalls of a
sacrificial layer that is subsequently removed.
Therefore, the sacrificial layer may be significantly
25   shorter than the first metal layer of the Co-pending
Application, with the spacer structures
correspondingly less thick. The reduced inter-pixel
spacing of the array permitted by this configuration
in turn permits fabrication of arrays having a
30   greater density of pixel cells and enhanced image
resolution. Thus, inter-pixel spacing of
approximately 0.05 μm can be achieved utilizing the
present invention.

Although the invention has been described in connection with one specific preferred embodiment, it must be understood that the invention as claimed should not be unduly limited to this embodiment.

5   Various other modifications and alterations in the structure and process will be apparent to those skilled in the art without departing from the scope of the present invention.

For example, as shown in FIG. 4CA, the

10 photoresist layer forming the first mask may be specifically patterned to exclude corners of the square portions, thereby providing space for dielectric material between diagonally-situated pixels. However, there are several possible

15 alternatives to this step.

FIG. 5 shows a plan view of a photoresist mask in accordance with a first alternative embodiment of the present invention. In FIG. 5, first mask 500 is formed by patterning a photoresist layer in a precise

20 checkerboard pattern, followed by carefully over-exposing the photoresist layer during development. As a result of this calculated over-exposure, corners 500a of first mask 500 are rounded and exclude corner portions 502.

25 FIG. 6 shows a plan view of a photoresist mask in accordance with a second alternative embodiment of the present invention. The exposure kinetics of a particular photolithography system may require surplus photoresist material in corner regions in

30 order to ensure that gaps are formed between diagonally-situated electrodes. Photoresist layer 600 therefore includes corner portions 602 linked together by tabs 604. Development of the patterned photoresist layer 604 may ultimately eliminate tabs

604 altogether, creating the necessary gaps to form between corners of diagonally-situated pixels.

Composition of the various layers making up the array may be varied to achieve optimum device performance and/or process efficiency. For example, FIGS. 4AA-4HB depict successive formation of first and second dielectric layers. These dielectric layers may be composed of silicon oxide, silicon nitride, or any other conforming dielectric material whose rates of formation and etching can be precisely controlled.

Furthermore, significant advances have recently been reported in creating materials having particularly low dielectric constants. Promising "low-k" dielectric materials include, but are not limited to, fluorosilicate glass (FSG), nanoporous silica, and organic polymers.

The thicknesses of the various layers of the array could also be varied and the array would still remain within the scope of the present invention. Thus, by employing low-k dielectric materials to provide inter-pixel isolation, thickness of the dielectric spacers may be decreased. This is because equivalent electrical isolation may be accomplished utilizing the same volume of dielectric material. Pixel arrays having even greater cell densities, higher resolution, and reduced light leakage between pixels may thus be formed in accordance with the present invention.

Finally, while FIG. 4HA-4HB depict chemical-mechanical polishing through the second dielectric layer into the metal layer to form the array, a number of alternatives to this step also exist.

For example, FIG. 7 shows a cross-sectional view of chemical-mechanical polishing in accordance with an alternative embodiment of the present invention. As shown in FIG. 7, chemical-mechanical polishing of

5   metal layer 700 could stop on lower portions of the second dielectric layer, with remaining dielectric material from second dielectric layer removed by wet etching. The relative size of the remaining metal topography is much exaggerated in FIG. 7, as the

10   actual pixel width would be much greater than illustrated.

The approach shown in FIG. 7 would protect the surface of the electrode from reflectance loss attributable to polishing. This approach would also

15   leave curved upper portions of the dielectric spacers largely intact, permitting even closer spacing between adjacent electrodes.

Another alternative chemical-mechanical polishing approach would be to dispense entirely with

20   the second dielectric layer, with the expectation that chemical-mechanical polishing of the metal layer would not overly degrade its reflectance.

Given the multitude of embodiments described above, it is therefore intended that the following

25   claims define the scope of the present invention, and that the methods and structures within the scope of these claims and their equivalents be covered hereby.